Hall Ticket Number:

Code No.: 22603 M

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD

M.E. (ECE: CBCS) II-Semester Make Up Examinations, September-2017

(Embedded Systems & VLSI Design)

Low Power VLSI Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from Part-B*

Part-A (10 × 2 = 20 Marks)

1. Write the list of parameters which affect power dissipation in a CMOS circuit.
2. Write the types of power dissipation in VLSI Circuits.
3. Explain the reverse leakage current paths in a CMOS inverter.
4. Discuss the importance of dynamic power dissipation in VLSI circuits.
5. How is software power estimation done?
6. List the implementation issues of adiabatic logic.
7. Compare current sense amplifier with a voltage sense amplifier in SRAMs.
8. Explain the operation of 6T-CMOS SRAM cell.
9. Compare parallel and pipelined implementation of architecture driven voltage scaling.
10. How low and high supply voltages are to be chosen according to the technology?

Part-B (5 × 10 = 50 Marks)

11. a) Write about sources of leakage power with neat diagram. [5]
    b) What is Drain Induced Barrier Lowering of NMOS transistor? How does it affect Power consumption? [5]

12. a) Discuss Memory Parallelization. [5]
    b) Draw the block diagram of a double-edge triggered flip-flop (DET-FF) and discuss how clock power reduction is achieved. [5]

13. a) Mention the available High-Throughput CMOS Circuit Techniques and discuss any two in brief. [6]
    b) Write briefly about sources of software power dissipation. [4]

14. a) Compare two low voltage low power SRAM cell designs. [6]
    b) Discuss the importance of Pre-charge and equalization circuits in SRAM structures. [4]

15. a) Discuss how power optimization is achieved using operation substitution. [6]
    b) Discuss the effect of voltage scaling on delay and threshold voltage. [4]

16. a) Discuss the principle of MTCMOS with an example. [5]
    b) What is transistor stacking? How does it help leakage power reduction? [5]

17. Answer any ***two*** of the following:
    a) Principle of adiabatic charging. [5]
    b) Design of a Static row decoder for a 128 KB SRAM. [5]
    c) Power reduction using dynamic supply voltage design. [5]